FERROELECTRIC CAPACITOR AND SEMICONDUCTOR DEVICE HAVING A FERROELECTRIC CAPACITOR

CROSS REFERENCE TO RELATED APPLICATION

A claim of priority under 35 U.S.C. §119 is made to Japanese Patent Application No. 2003-024772, filed January 31, 2003, which is herein incorporated by reference in its entirety for all purposes.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a ferroelectric capacitor and a semiconductor device having a ferroelectric capacitor.

DESCRIPTION OF THE RELATED ART

A FeRAM(ferroelectric random access memory) uses a ferroelectric capacitor. Data can be read quickly from the FRAM, which can be operated to provide random access. Therefore, the FeRAM is expected as a new type of nonvolatile memory.

A memory cell of the FeRAM includes a switching transistor and a ferroelectric capacitor. The FeRAM uses a function of the ferroelectric layer for reversing an electric field by an intrinsic polarization and for retaining the electric field.

The FeRAM is classified broadly into ether a planar type or a stack type. In the

planar type FeRAM, a top electrode of the ferroelectric capacitor is connected to a source electrode of a corresponding switching transistor.

In the stack type FeRAM, a bottom electrode of the ferroelectric capacitor is connected to the source electrode of the switching transistor via a conductive plug. Therefore, an area of a memory cell of the stack type FeRAM is smaller than an area of a memory cell of the planar type FeRAM. Such technique is shown in a "A FRAM technology using 1T1C and triple metal layers for high performance and high density FRAMs", S. Y. Lee et al., 1999 Symposium on VLSI Technology Digest of Technical Papers, 1999, pp. 141-142. Alternatively, a FeRAM structure that has a cross-sectional area of a bottom electrode smaller than a cross-sectional area of a ferroelectric layer is described in Japanese Patent Laid-Open No 2001-308287.

In the conventional FeRAM, a bottom electrode layer, a ferroelectric layer and a top electrode layer are formed in order, and then, these layers are etched all at once. However, a damaged layer might be formed on a side surface of the ferroelectric layer. The damaged layer is made by a reaction between a material of the ferroelectric layer, the top electrode or the bottom electrode and etching gas. If a damaged layer is formed, normal operation of the ferroelectric capacitor might be inhibited and reliability of the ferroelectric capacitor might not be ensured.

For solving the above problem, an alternative fabricating process for fabricating the FeRAM device is as follows. First, the bottom electrode layer is formed, and then the bottom electrode layer is etched to form the bottom electrode. Then, the ferroelectric layer is formed on the bottom electrode and the top electrode layer is formed on the

ferroelectric layer. Then, the ferroelectric layer and the top electrode layer are etched to form the ferroelectric capacitor.

However, in the FeRAM device which is fabricated by these above steps, oxygen is diffused in an insulating layer formed under the bottom electrode, while the ferroelectric layer is formed under an oxygen atmosphere. As a result, a plug which is embedded in the insulating layer is oxidized and a connection between the bottom electrode and a source electrode of a switching transistor might be disconnected.

Also, a process that reestablishes the function of the ferroelectric layer by cleaning the damaged layer has been considered. However, an amount of remaining polarization is not increased after the cleaning. Such process therefore is not an effective solution.

SUMMARY OF THE INVENTION

Accordingly, in one aspect of the present invention, a ferroelectric capacitor for reducing an influence of a damaged layer is provided. The ferroelectric capacitor includes a bottom electrode which has a projecting portion, a top electrode, a ferroelectric layer and a dielectric layer formed between the bottom electrode and the top electrode. The dielectric layer is formed on a peripheral area of the bottom electrode. The ferroelectric layer is formed on the dielectric layer and on the projecting portion of the bottom electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view showing a semiconductor device of a first

embodiment of the present invention.

Fig. 2 is a plane view showing the semiconductor device of the first embodiment of the present invention.

Figs. 3(A) to 3(C) are views showing manufacturing steps for a semiconductor device of the first embodiment of the present invention.

Figs. 4(A) and 4(B) are views showing a manufacturing steps for a semiconductor device of the first embodiment of the present invention.

Figs. 5(A) to 5(C) are views showing a ferroelectric capacitor of the first embodiment of the present invention.

Fig. 6 is a cross-sectional view showing a semiconductor device of a second embodiment of the present invention.

Figs. 7(A) to 7(C) are views showing manufacturing steps for a semiconductor device of the second embodiment of the present invention.

Fig. 8 is a cross-sectional view showing a semiconductor device of a third embodiment of the present invention.

Figs. 9(A) to 9(C) are views showing manufacturing steps for a semiconductor device of the third embodiment of the present invention.

Fig. 10 is a cross-sectional view showing a semiconductor device of a fourth embodiment of the present invention.

Fig. 11 is a plane view showing the semiconductor device of the fourth embodiment of the present invention.

Figs. 12(A) to 12(C) are views showing manufacturing steps for a semiconductor

device of the fourth embodiment of the present invention.

Figs. 13(A) to 13(C) are views showing manufacturing steps for a semiconductor device of the fourth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A semiconductor device according to preferred embodiments of the present invention will be explained hereinafter with reference to the accompanying figures. In order to simplify the explanation, like elements are given like or corresponding reference numerals. Dual explanations of the same elements are avoided.

First preferred embodiment

Fig. 1 is a cross-sectional view showing a semiconductor device 10 of a first embodiment of the present invention. The semiconductor device 10 as shown in Fig. 1 is a cross-sectional view taken along line 1-1' in Fig. 2. In this embodiment, a stack type FeRAM is described.

Initially, the semiconductor device 10 is explained in reference to Fig. 2. A memory cell 50 of the semiconductor device 10 includes a MOSFET(Metal Oxide Semiconductor Field Effect Transistor) 20 and a ferroelectric capacitor 60 as shown in Fig. 2. The transistor 20 includes a source region as a first region 24 and a drain region as a second region 26 and a gate electrode as a control electrode 22. The first region 24 and the second region 26 are formed in an active area 30 and the gate electrode 22 is arranged on an area which is located between the first region 24 and the second region 26. The gate electrode 22 is used as a word line in the semiconductor device 10. The drain region 26 is

connected to a bit line 55 via a bit line contact 32. The source region 24 is connected to a bottom electrode 62 of the ferroelectric capacitor 60 via a plug 34. The ferroelectric capacitor 60 includes a ferroelectric layer 64 formed between the bottom electrode 62 and a top electrode 66. The top electrode 66 is connected to the plate line 57 via a plate contact 36. In this type of the semiconductor device, bit line 55 is extended in a direction perpendicular to each of the gate electrode 22 and the plate line 57.

Then, the device structure of the semiconductor device 10 is explained in reference to Fig. 1. The transistor 20 includes the gate electrode 22, the source region 24 and the drain region 26 as shown in Fig. 1. The gate electrode 22 is formed on the silicon substrate 12 via a gate insulating layer(not shown). The source region 24 and the drain region 26 are formed in the semiconductor substrate 12 located at both sides of the gate electrode 22. An insulating layer 13 such as silicon dioxide is formed on the transistor 20 and the silicon substrate 12, and a top surface of the insulating layer is flattened.

The source region 24 is connected to the bottom electrode 62 via the plug 34 which is formed in the insulating layer 13. The plug 34 is formed by embedding a conductive material such as poly crystalline silicon or tungsten in a contact hole 14 which is formed in the insulating layer 13. Further, a barrier metal 17 such as titanium nitride or aluminum nitride is formed between the plug 34 and the bottom electrode 62. The barrier metal 17 inhibits a counter diffusion of the metal. The barrier metal 17 can be formed in the contact hole 14. Also, an adhesive layer such as a titanium dioxide layer for improving an adhesion between the barrier metal 17 and the bottom electrode 62 can be used.

The drain region 26 is connected to a bit line 55 such as tungsten or tungsten

silicide via a bit line contact 32 which is formed in the insulating layer 13. The bit line contact 32 is formed by embedding a conductive material such as poly crystalline silicon or tungsten in a contact hole 14 which is formed in the insulating layer 13. An insulating layer 19 divides the adjacent transistors.

The ferroelectric capacitor 60 includes the bottom electrode 62 formed on the barrier metal 17, a dielectric layer 63 formed on the bottom electrode 62, the ferroelectric layer 64 formed on the bottom electrode 62 and the dielectric layer 63,and the top electrode 66 formed on the ferroelectric layer 64. The bottom electrode 62 includes a plate portion 62a and a projection portion 62b formed on a surface "a" of the plate portion 62a. The plate portion 62a and the projection portion 62b are made of platinum. The projection portion 62b is located at a central area of the surface "a" of the plate portion 62a. The dielectric layer 63 is formed around the projection portion 62b and a top surface of the dielectric layer 63 is aligned or substantially coplanar with a top surface "b" of the projection portion 62b. The dielectric layer 63 is made of silicon dioxide or silicon nitride. The ferroelectric layer 64 is formed on the top surface "b" of the projection portion 62b and on the dielectric layer 63. The ferroelectric layer 64 is made of strontium bismuth tantalate ($SrBi_2Ta_2O_9$). The top electrode 66 is formed on the ferroelectric layer 64 and is made of platinum.

In this embodiment, the capacitor 60 is rectangular in shape. Also, the projection portion 62a is rectangular in shape. Each side of the projection portion 62b of the bottom electrode 62 is shorter than corresponding side of the plate portion 62a of the bottom electrode 62. A side surface "e" of the plate portion 62a, a side surface "f" of the

dielectric layer 63, a side surface "g" of the ferroelectric layer 64 and a side surface "h" of the top electrode 64 are aligned with each other.

In the alternative, a side surface of the projection portion 62b can be formed in a forward tapered shape. Preferably, an angle θ between the surface "a" of the plate portion 62a and the side surface "c" of the projection portion 62b ranges from 70° to 80° so that the projection portion 62b can be easily formed. The top electrode 66 and the bottom electrode 62 can be made of oxidation resistance metal such as iridium(Ir), ruthenium(Ru) or strontium ruthenium oxide($SrRuO_3$), or conductive metal oxide such as iridium oxide(IrO_2) or ruthenium oxide(RuO_2). The ferroelectric layer 64 can be made of lead zirconate titanate($PbZrTiO_3$), lanthanum (La), lead zirconate titanate doped with lanthanum, strontium bismuth tantalate doped with niobium or bismuth lanthanum titanate($LaBiTiO_3$). These materials are applicable in following embodiment.

The ferroelectric capacitor 60 is formed in an insulating layer 16 such as silicon dioxide. A top surface of the insulating layer 16 is flattened and aligned to a top surface of a plate line contact 36 such as tungsten which is formed on the top electrode 66. The top electrode 66 is connected to a plate line 57 such as aluminum via the plate line contact 36.

Next, a method of fabricating the semiconductor device 10 is explained with reference to Figs. 3(A) to 3(C) and Figs. 4(A) and 4(B).

First, as shown in Fig. 3(A), the insulating layer 19, the transistor 20, bit line contact 55 and the bit line 55 are formed on the semiconductor substrate 12. Then, the insulating layer 13 is formed on the semiconductor substrate 12 and the top surface of the

insulating layer 13 is flattened by a CMP(Chemical Mechanical Polishing) technique.

Then, another contact hole 14 for the capacitor is formed in the insulating layer 13. A tungsten layer is formed in the contact hole 14 and on the insulating layer 13. Then, for forming the plug 34, the tungsten layer is polished by the CMP technique so as to align with the top surface of the insulating layer 13.

Then, the barrier metal 17 that has 70nm thickness such as titanium nitride is formed on the insulating layer 13 by reactive sputtering technique. The barrier metal 17 contacts the top surface of the plug 34.

Then, as shown in Fig. 3(B), a platinum layer 65 that has 150nm thickness is formed on the barrier metal 17 by a sputtering technique.

Then, a mask M1 such as silicon nitride or titanium nitride is formed on the platinum layer 65. The platinum layer 65 is etched by using the mask M1 so that the projection portion 62b is formed. For example, a size of the projection portion 62b is 1040nm by 800nm and a thickness is 75nm. In this step, a bottom electrode layer 67 which has the projection portion 62b formed on a platinum layer 67a is obtained.

Then, as shown in Fig. 3(C), a dielectric layer 68 is formed on the bottom electrode 67 and the dielectric layer 68 is etched back so that the top surface "b" of the projection portion 62b is exposed from the dielectric layer 68. As a result, a top surface of the dielectric layer 68 is aligned to the top surface "b" of the projection portion 62a.

Then, a strontium bismuth tantalate solution is supplied on the dielectric layer 68 and the projection portion 62a by a spin coat method. After the solution is dried, the dried solution is annealed in an oxygen atmosphere at 700°C for one minute by an RTA(Rapid

Thermal Anneal) method. As a result, a strontium bismuth tantalate layer that has 50nm thickness is obtained. Then, the coating step and the RTA step are again performed another two times at 750°C for one minute, as shown in Fig. 4(A). As a result, a 150nm thickness strontium bismuth tantalate layer 69 is obtained.

Then, a 100nm thickness platinum layer 61 as the top electrode layer is formed on the strontium bismuth tantalate layer 69 by a sputtering method. Then, a mask M2 such as silicon dioxide is formed on the top electrode layer 61 as further shown in Fig. 4(A). A size of the mask M2 is 1300nm by 1000nm, and the mask M2 is arranged so that a distance from each side of the projection portion 62a to corresponding sides of the mask M2 will be equal.

Then, the top electrode layer 61, the ferroelectric layer 69, the dielectric layer 68, the plate portion 67a of the bottom electrode layer 67, and the barrier metal 17 are etched by using the mask M2 so that the side surface "e" of the plate portion 62a, the side surface "f" of the dielectric layer 63, the side surface "g" of the ferroelectric layer 64 and the side surface "h" of the top electrode 66 are aligned. Then the mask M2 is removed and the ferroelectric capacitor 60 is obtained as shown in Fig. 4(B).

In this embodiment, a photomask which is used for exposing a photoresist to form the mask M2 can be the same photomask which is used for exposing a photoresist to form the mask M1. If an exposing amount is changed, an exposed area is changed. In this embodiment, an exposing amount of the photoresist for forming the mask M1 is greater than an exposing amount of the photoresist for forming the mask M2.

Then, the insulating layer 16 is formed on the ferroelectric capacitor 60. The top

surface of the insulating layer 16 is flattened by the CMP technique. Then, a contact hole 31 is formed in the insulating layer 16 so as to expose the top electrode 66. After a tungsten layer is formed in the contact hole 31 and on the insulating layer 16, the tungsten layer is polished so as to remove the tungsten layer which is formed on the insulating layer 16. The remaining tungsten layer is plate line contact 36. Then, the plate line 57 such as aluminum is formed on the plate line contact 36.

In this embodiment, the bottom electrode layer 67, the dielectric layer 68, the ferroelectric layer 69 and the top electrode layer 61 are etched as shown in Fig. 4(A) by using the common mask M2. In the alternative, the top electrode layer 61 can be formed after the bottom electrode 62, the dielectric layer 63 and the ferroelectric layer 64 are formed.

An effective area of the ferroelectric capacitor is explained with reference to Fig. 5(A) to Fig. 5(C). Fig. 5(A) shows a cross-sectional view showing the ferroelectric capacitor 60. Fig. 5 (B) is a plane view taken along line 5(B)-5(B)' in Fig. 5(A). Fig. 5(C) is a equivalent circuit of the ferroelectric capacitor 60.

In this embodiment, the effective area 601 of the ferroelectric capacitor 60 is an area which includes the projection portion 62b, an area 66a of the top electrode which faces the projection portion 62b, and an area 64a of the ferroelectric layer 64 which is located between the projection portion 62b and the area 66a as shown in Fig. 5(A) and Fig. 5(B).

A thickness of the ferroelectric layer 64 is shown as "t_{fe}" and a thickness of the dielectric layer 63 is shown as "t_{ox}".

The ferroelectric capacitor 60 includes a ferroelectric capacitor C_{fe0} in the effective

area 601 and a dielectric capacitor C_{ox} in a spacer area 602. The dielectric capacitor Cox includes the dielectric layer 63 and a corresponding part of the bottom electrode 62aa and the top electrode 66b. A ferroelectric capacitor C_{fe1} includes a ferroelectric layer 64b which corresponds to the dielectric layer 63, and a corresponding part of the top electrode 66b and the bottom electrode 62aa.

Fig. 5(c) shows a connection of each capacitor. The ferroelectric capacitor C_{fe1} and the dielectric capacitor C_{ox} are connected serially. The ferroelectric capacitor C_{fe0} is connected to these serial connected capacitors C_{fe1} and C_{ox} in parallel. The connection of the ferroelectric capacitor C_{fe0}, the ferroelectric capacitor C_{fe1} and the dielectric capacitor C_{ox} are electrically equal to the ferroelectric capacitor 60.

Therefore, a capacitance "D" of the ferroelectric capacitor 60 is shown in the following equation (1). In the following equation, a capacitance of the ferroelectric capacitor C_{fe0} is shown as D_{fe0}, a capacitance of the ferroelectric capacitor C_{fe1} is shown as D_{fe1} and a capacitance of the dielectric capacitor C_{ox} is shown as D_{ox}.

$$D = D_{fe0} + (D_{fe1} * D_{ox}) / (D_{fe1} + D_{ox}) \quad (1)$$

The effective area 601 has a size of m_1 by m_2 and a width of d1 along the short sides of the rectangular shaped area of the capacitor structure and a width of d2 along the longer sides of the rectangular shaped area. A dielectric constant of the ferroelectric layer 64 is shown as ε_{fe}, a dielectric constant of the dielectric layer 63 is shown as ε_{ox}. A capacitance of each capacitor is shown in the following equations.

$$D_{fe0} = (\varepsilon_{fe} * m_1 * m_2) / t_{fe} \quad (2)$$

$$D_{fe1} = 2\varepsilon_{fe} (m_2 * d_1 + m_1 * d_2 + 2d_1 * d_2) / t_{ox} \quad (3)$$

$$D_{ox} = 2\varepsilon_{ox} (m_2 * d_1 + m_1 * d_2 + 2d_1 * d_2) / tox \quad (4)$$

The thickness t_{fe} and the thickness t_{ox} are 150nm. A voltage of 3V is applied to the ferroelectric capacitor 60. The dielectric constant ε_{fe} of strontium bismuth tantalate as the ferroelectric layer 64 is forty times larger than the dielectric constant ε_{ox} of silicon dioxide as the dielectric layer 63.

As a result, a voltage of 3V is applied to the effective area of the ferroelectric capacitor C_{fe0}. However, a voltage of 0.075V, which is 1/40 of the voltage applied to, is applied to the dielectric capacitor C_{ox}, is applied to the spacer area of the ferroelectric capacitor C_{fe1}.

The ferroelectric capacitor C_{fe1} does not exhibit a hysteresis characteristic under the voltage of 0.075V. Therefore, the capacitance of the spacer area 602 is substantially the same as the capacitance of the dielectric capacitor C_{ox}. As a result, the capacitance D of the ferroelectric capacitor 60 is as shown in the following equation (5).

$$D = Dfe0 + (Dfe1 * Dox) / (Dfe1 + Dox) = D_{feo} + D_{ox} \quad (5)$$

The leakage of a charge caused by the spacer area 602 can be ignored. The reason is explained as follows.

For example, the size of the top electrode 66 and the size of the plate portion 62a of the bottom electrode 62 are 1300nm by 1000nm and each width of the spacer d_1 and d_2 are 10% of each side. That is, m_1 is 1040nm, m_2 is 800nm, d_2 is 130nm and d_1 is 100nm.

In reference to equations (2), (4) and (5), the capacitance D_{ox} of the spacer area 602 is 1/80 of the capacitance D of the ferroelectric capacitor 60. In the alternative, if lead zirconate titanate is used as the ferroelectric layer 63, the capacitance D_{ox} of the spacer

area is 1 / 320 of the capacitance D of the ferroelectric capacitor 60.

In this embodiment, the effective area of the ferroelectric capacitor is the same as the area of the top surface of the projection portion 62b. Therefore, the damage area which is formed on the side surface of the ferroelectric layer 64 is arranged at the spacer area which is out of the effective area. That is, since the dielectric layer 63 decreases an electric field strength at a peripheral area of the capacitor, an influence of the damaged layer can be ignored.

In this embodiment, the step of forming the ferroelectric layer 69 in an oxygen atmosphere is performed on the bottom electrode layer 67 which has a function of oxidation resistance. Therefore, an oxidation of the plug 34 is inhibited by the bottom electrode 67.

Second preferred embodiment

In the second embodiment, a projection portion 72a of a bottom electrode 72 and a plate portion 72b of the bottom electrode 72 are made of different material as shown in Fig. 6.

In this embodiment, the bottom electrode 72 of a ferroelectric capacitor 70 includes the plate portion 72a such as iridium and the projection portion 72b such as iridium oxide.

Next, a method of fabricating a semiconductor device 200 is explained in reference with Fig. 7.

From the step for forming the transistor 20 to the step for forming plug 34 are performed as described in the first embodiment.

Then, the iridium layer 71 which has 100nm thickness is formed on the barrier metal 17 by a sputtering technique. Then, the iridium oxide layer 73 which has 100nm

thickness is formed on the iridium layer 71 by a reactive sputtering technique as shown in Fig. 7(A). The iridium layer 71 and the iridium oxide layer 73 form a conductive layer 74 for forming the bottom electrode.

Then, the iridium oxide layer 73 is etched so that the projection portion 72b is formed and the iridium layer 71a is exposed, as shown in Fig. 7(B). The iridium oxide layer 73 is etched by a mixed gas of chlorine(Cl) and oxygen(O_2).

In this step, a bottom electrode layer 78 which has a projection portion 72b is obtained as shown in Fig. 7(B).

Then, the dielectric layer, the ferroelectric layer and the top electrode layer are formed and the etching step is performed as described in the first embodiment, as shown in Fig. 7(C). The side surface "e" of the plate portion 72a, the side surface "f" of the dielectric layer 63, the side surface "g" of the ferroelectric layer 64 and the side surface "h" of the top electrode 66 are aligned. In the alternative, a combination of the projection portion 72b and the plate portion 72a can be selected from a combination of Pt/IrO_2, Ru/Ir, Ru/IrO_2, RuO_2/Ir and RuO_2/IrO_2.

Accordingly, since the bottom electrode layer 72 is made of two stacked layers of different material, an end point of etching for forming the projection portion 72b is found easily. Therefore, the projection portion 72b is formed with accuracy.

Third preferred embodiment

Fig. 8 is a cross-sectional view showing a semiconductor device 300 of a third embodiment of the present invention. Figs. 9(A) to (C) are views showing manufacturing steps for a semiconductor device 300 of the third embodiment of the present invention.

The bottom electrode 82 includes a stacked plate portion 82a and a projection portion 82b such as platinum formed on the stacked plate portion 82a. The stacked plate portion 82a includes an iridium layer 821 as a lower layer and an iridium oxide layer 822 as an upper layer.

The iridium oxide layer 822 has good adhesive characteristic for adhering to the platinum projection portion 82b. The iridium layer 821 has a function for resisting oxidation. As a result, an end point of etching for forming the projection portion 82b is found easily, and the platinum projection portion 82b can be used. That is, the platinum projection portion 82b which improves a capacitor characteristic and the iridium layer 821 can be used as the bottom electrode 82 without peeling of layers.

Then, the manufacturing steps are explained in reference with Figs. 9(A) to (C).

From the step for forming the transistor 20 to the step for forming the plug 34 are performed as described in the first embodiment.

Then, a conductive layer 84 as shown in Fig. 9(A) is formed as following steps. An iridium layer 81 having 100nm thickness is formed on the barrier metal 17 by a sputtering technique, an iridium oxide layer 83 having 50nm thickness is formed on the iridium layer 81 by a reactive sputtering technique, and a platinum layer 85 having 100nm thickness is formed on the iridium oxide layer 83 by a sputtering technique.

Then, the platinum layer 85 is etched so that the projection portion 82b is formed and the iridium oxide layer 83 is exposed. The platinum layer 85 is etched by a mixed gas of chlorine(Cl) and argon(Ar). In this step, a bottom electrode layer 88 which has a projection portion 82b is obtained as shown in Fig. 9(B).

Then, the dielectric layer, the ferroelectric layer and the top electrode layer are formed and the etching step is performed as described in the first embodiment as shown in Fig. 9(C). The side surface "e" of the plate portion 82a, the side surface "f" of the dielectric layer 63, the side surface "g" of the ferroelectric layer 64 and the side surface "h" of the top electrode 66 are aligned. In the alternative, a combination of the projection portion 82b/the upper side of the plate portion 822/the under side of the plate portion 821 can be selected from a combination of $Ir/IrO_2/Ir$, $Ru/IrO_2/Ir$ and $Ru/RuO_2/Ir$.

The bottom electrode such as platinum has a good ferroelectric characteristic. In this embodiment, the platinum bottom electrode can be used without peeling.

Fourth preferred embodiment

Fig. 10 is a cross-sectional view showing a semiconductor device 500 of a fourth embodiment of the present invention. Fig. 11 is a plane view showing the semiconductor device 500 of the fourth embodiment of the present invention. Also, the semiconductor device 500 as shown in Fig. 10 is a cross-sectional view taken along line 10-10' in Fig. 11. In this embodiment, a planar type FeRAM is described.

Initially, the semiconductor device 500 is explained in reference to Fig. 11. A memory cell 300 of the semiconductor device 500 includes the transistor 20 and a ferroelectric capacitor 90 as shown in Fig. 11. The transistor 20 includes the source region as the first region 24 and a drain region as the second region 26 and the gate electrode as the control electrode 22. The first region 24 and the second region 26 are formed in the active area 30 and the gate electrode 22 is arranged on the area which is located between the first region 24 and the second region 26. The gate electrode 22 is used as the word line in

the semiconductor device 500. The drain region 26 is connected to the bit line 55 via the bit line contact 32. The source region 24 is connected to one end of a wiring 39 via a contact plug 37. The ferroelectric capacitor 90 includes a ferroelectric layer 94 formed between the bottom electrode 92 and a top electrode 96. The top electrode 96 is connected to the other end of the wiring 39 via a contact hole 40.

Then, the device structure of the semiconductor device 500 is explained in reference to Fig. 10. The transistor 20 includes the gate electrode 22, the source region 24 and the drain region 26 as shown in Fig. 10. The gate electrode 22 is formed on the silicon substrate 12 via a gate insulating layer(not shown). The source region 24 and the drain region 26 are formed in the semiconductor substrate 12 located at both sides of the gate electrode 22. The insulating layer 13 such as silicon dioxide is formed on the transistor 20 and the silicon substrate 12, and the top surface of the insulating layer is flattened.

The source region 24 is connected to the contact plug 37 and the drain region 26 is connected to the bit line contact 32. The contact plug 34 and the bit line contact 32 are formed by embedding a conductive material such as poly crystalline silicon or tungsten in contact holes 33 which are formed in the insulating layer 13.

The ferroelectric capacitor 90 includes the bottom electrode 92 formed on an adhesive layer 11 such as titanium oxide, a dielectric layer 93 formed on the bottom electrode 92, the ferroelectric layer 94 formed on the bottom electrode 92 and the dielectric layer 93,and the top electrode 96 formed on the ferroelectric layer 94. The bottom electrode 92 includes a plate portion 92a and a projection portion 92b formed on a surface

"a" of the plate portion 92a. The plate portion 92a includes an iridium layer 921 formed on the adhesive layer 11 and an iridium oxide layer 922 formed on the iridium layer 921. The projection portion 92b is made of platinum. The projection portion 92b is located at a central area of the surface "a" of the plate portion 92a. The dielectric layer 93 is formed around the projection portion 92b and a top surface of the dielectric layer 93 is aligned to a top surface "b" of the projection portion 92b. The dielectric layer 93 is made of silicon dioxide or silicon nitride. The ferroelectric layer 94 is formed on the top surface "b" of the projection portion 92b and on the dielectric layer 93. The ferroelectric layer 94 is made of strontium bismuth tantalate ($SrBi_2Ta_2O_9$). The top electrode 96 is formed on the ferroelectric layer 94 and is made of platinum.

In this embodiment, the plate portion 92a of the bottom electrode 92 is used as a plate line of the semiconductor device 500. That is, the plate portion 92a of the bottom electrode 92 has a line shaped and a plurality of the ferroelectric capacitors 90 share the common plate portion 92a. Also, the ferroelectric layer 94 has a line shaped and is formed on the bottom electrode 92 so as to extend along the bottom electrode 92. Each of the top electrodes 96 is formed on the respective ferroelectric capacitor 90 separately so as to cover the projection portion 92a of the each bottom electrode 92.

In this embodiment, the capacitor 90 is rectangular in shape. Also, the projection portion 92a is rectangular in shape. Each side of the projection portion 92b of the bottom electrode 92 is shorter than corresponding side of the plate portion 92a of the bottom electrode 92. A side surface "e" of the plate portion 92a, a side surface "f" of the dielectric layer 93, a side surface "g" of the ferroelectric layer 94 and a side surface "h" of

the top electrode 96 are aligned with each other.

The insulating layer 16 such as silicon dielectric has contact holes 23. The contact plug 37 and the bit line contact 32 are exposed in the contact holes 23. The top electrode 96 of the ferroelectric capacitor 90 and the source region 24 of the transistor 20 are connected by the wiring 39. The drain region 26 of the transistor 20 is connected to a bit line 55 via the bit line contact 32.

Next, a method of fabricating the semiconductor device 500 is explained with reference to Figs. 12(A)-12(C) and Figs 13(A)-13(C).

First, as shown in Fig. 12(A), a plurality of transistors 20 and the insulating layer 13 are formed on the semiconductor substrate 12 as the same method of the first embodiment. Then, contact holes 33 are formed in the insulating layer 13. A tungsten layer is formed in the contact holes 33 and on the insulating layer 13. Then, for forming the plug 37 and the bit line contact 32, the tungsten layer is polished by the CMP technique so as to align with the top surface of the insulating layer 13.

Then, the adhesive layer 11 such as titanium oxide which has 70nm thickness is formed on the insulating layer 13 by the reactive sputtering technique.

Then, a conductive layer 99 is formed in the following steps. An iridium layer 91 having 100nm thickness is formed on the adhesive layer 11 by a sputtering technique, an iridium oxide layer 97 which has 50nm thickness is formed on the iridium layer 91 by a reactive sputtering technique, and a platinum layer 98 which has 100nm thickness is formed on the iridium oxide layer 97 by a sputtering technique.

Then, the platinum layer 98 is etched so that the projection portion 92b is formed

and the iridium oxide layer 97 is exposed. The platinum layer 98 is etched by a mixed gas of chlorine(Cl) and argon(Ar). In this step, a bottom electrode layer 102 which has a projection portion 92b is obtained as shown in Fig. 12(B).

Then, a dielectric layer 101 is formed on the bottom electrode 102 and the dielectric layer 101 is etched back so that the top surface "b" of the projection portion 92b is exposed from the dielectric layer 101. As a result, a top surface of the dielectric layer 101 is aligned to the top surface "b" of the projection portion 92b as shown in Fig. 12(C).

Then, a strontium bismuth tantalate solution is supplied on the dielectric layer 101 and the projection portion 92a by a spin coat method. After the solution is dried, the dried solution is annealed in an oxygen atmosphere at 700°C for one minute by an RTA method. As a result, a strontium bismuth tantalate layer that has 50nm thickness is obtained. Then, the coating step and the RTA step are performed two further times at 750°C for one minute. As a result, a 150nm thickness strontium bismuth tantalate layer 104 is obtained, as shown in Fig. 13(A).

Then, a 100nm thickness platinum layer 106 as the top electrode layer is formed on the strontium bismuth tantalate layer 104 by the sputtering method as further shown in Fig. 13(A). Then, the top electrode layer 108, the ferroelectric layer 104, the dielectric layer 101 and the plate portion 95 of the bottom electrode layer 102 are etched so as to form a ferroelectric structure 110 as shown in Fig. 13(B). The side surface "e" of the plate portion 92a, the side surface "f" of the dielectric layer 93, the side surface "g" of the ferroelectric layer 94 and the side surface "h" of the top electrode 108 are aligned.

Then, the top electrode 108 is etched so as to obtain the separated top electrodes 96

as shown in Fig. 13(C).

Then, the insulating layer 16 such as silicon dioxide is formed on the ferroelectric capacitor 90 by a CVD technique. Then, the contact holes 23 are formed in the insulating layer 16. Then, the wiring 39 for connecting the separated top electrode 96 to the corresponding contact plug 37 and the bit line 55 for connecting to the bit line contact 32 are formed.

In this embodiment, the effective area of the ferroelectric capacitor is the same as the area of the top surface of the projection portion 92b. Therefore, the damage area which is formed on the side surface of the ferroelectric layer 90 is arranged at the spacer area which is out of the effective area.

While the preferred form of the present invention has been described, it is to be understood that modifications will be apparent to those skilled in the art without departing from the spirit of the invention. The scope of the invention is to be determined solely by the following claims.